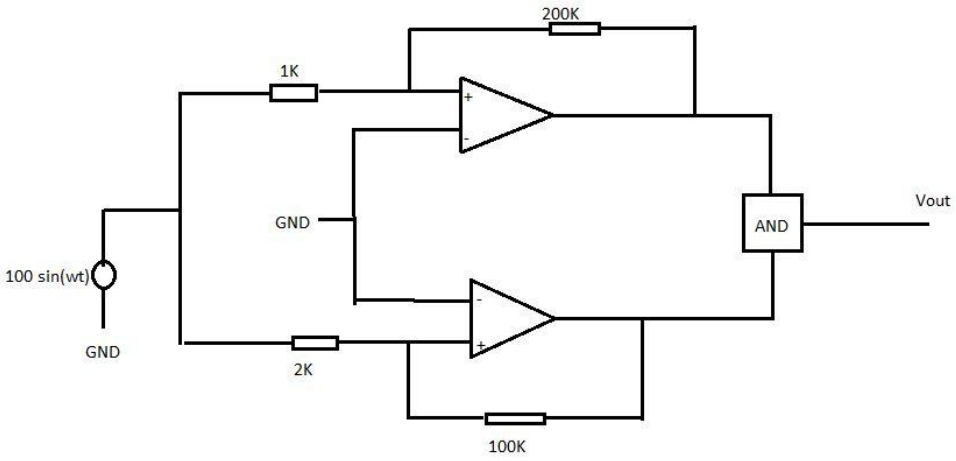
FREESCALE SEMICONDUCTOR MNNIT Campus Visit 20-21 Jan 14

This question paper is based on memory…. However we have tried our best to recollect all the data as far as possible…

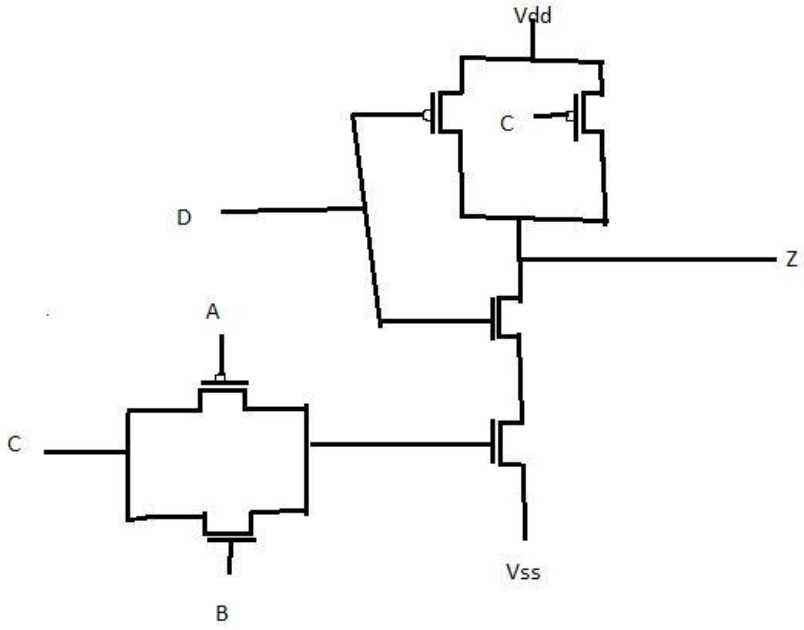
Question paper consists of 12 subjective questions of 80 marks. Time allotted was 90 min.

Q.1 In the given fig. draw the output waveform. Saturation voltages for op-amp are 5V and 0V.

Input signal is 100sin(wt) mV.

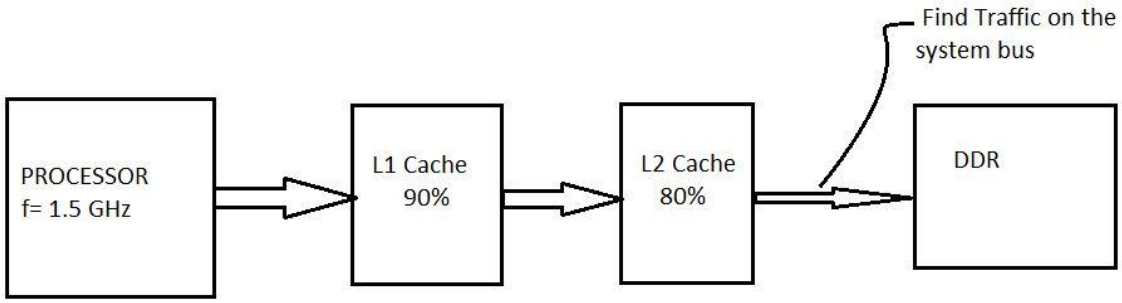


Q.2 Find the issues related with the following circuit.



Q.3 In the fig shown below. Find the traffic on the system bus. L1 and L2 are the cache memories associated with processor having hit ratios of 90% and 80% respectively.

[Hint: Assume that only one read signal is asserted in each cycle].



(Actual question was slightly different.This question was asked to me in interview during paper discussion)

Q.4 A logic function was implemented in SOP form using AND & OR gates. You have to simplify the expression so obtained using K-map.

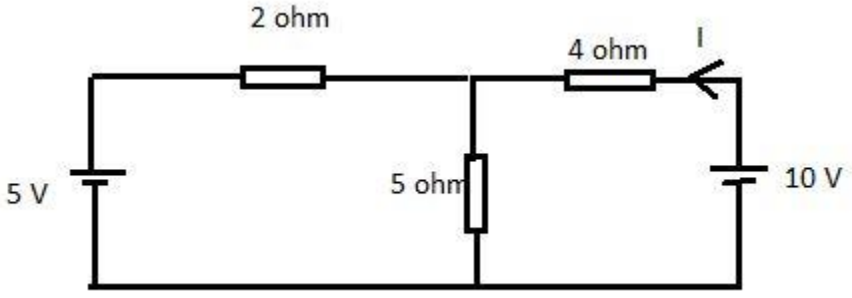
Q.5 Find the switching activity factor (transition probability from 0 to 1) for XOR gate. If the probabilities of two signals being logic '1' are P_a and P_b.

Q.6 Verilog based question:

(a) Reverse a 4-bit vector without using temporary register.

(b) write code for synchronous and asynchronous reset.

Q.7 (a) In the given circuit find current I through 4 ohm resistor using Thevenins theorem.



(b) Two RLC series circuit with same value of R and different values of L and C were given.

L and C values were such that they both had same resonant frequencies.

Resonant curves were drawn We were asked to match the plots with the given circuits.

Q.8 This question was based on Shannon Hartley Law (Shannon's Capacity Theorem). Signal Bandwidth and channel capacity was given and we were asked to calculate SNR and minimum no of levels required to attain this value of SNR.

Q.9 This question was based on set up time violation. The circuit included 3 flip flops, 3 inputs and a 2-stage synchronizer and some combinational logic in between 1^{st} and 3^{rd} & 2^{nd} and 3^{rd} flipflop. We were asked to check setup violation for all 3 inputs. Two inputs were delayed wrt to clock.

Q.10 Design a cicuit with the help of 3 bit counter which can count the no of 0's and no of 1's in the serial bit stream.

Q.11 Design a D flipflop using 2 X 1 MUX.

Q.12 A circuit using gates with different propagation delays was given. A delay element X was inserted to remove the glitch from the circuit. Find the delay of X.